

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method for mapping platform-based design to multiple foundry processes, comprising:
 - (a) predefining a slice, said slice being a constrained and abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, and a transistor array of a chip;
 - (b) mapping said slice onto a first fabrication process with a first set of design rules to produce a first result;
 - (c) evaluating said slice with a second fabrication process with a second set of design rules to produce a second result; and
 - (d) comparing said first result and said second result to produce a third result.
2. (original): The method of claim 1, wherein said slice is a RapidSlice™.
3. (original): The method of claim 1, wherein said step (d) is a hybrid analysis whereby evaluation of an element of said slice is discontinued when said element is established to be accessible in said second fabrication process.
4. (original): The method of claim 1, wherein said step (d) is accomplished with a network-distributed processing system.
5. (original): The method of claim 1, wherein said third result including at least one variable that is invariant in said platform-based design.
6. (original): The method of claim 1, further comprising modifying said slice definition based on said third result.

7. (original): The method of claim 1, further comprising optimizing a metalization process giving a final function of said slice based on said third result.
8. (original): The method of claim 1, further comprising modifying said first fabrication process based on said third result.
9. (original): The method of claim 1, further comprising modifying said second fabrication process based on said third result.
10. (original): The method of claim 1, further comprising storing said third result into a database.
11. (original): The method of claim 1, further comprising optimizing platform architecture used to predefine said slice based on said third result.
12. (original): The method of claim 11, further comprising optimizing temporal structure of interconnect of said platform architecture based on said third result.
13. (currently amended): An apparatus for mapping platform-based design to multiple foundry processes, comprising:
 - (a) means for predefining a slice, said slice being a constrained and abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, and a transistor array of a chip;
 - (b) means for mapping said slice onto a first fabrication process with a first set of design rules to produce a first result;
 - (c) means for evaluating said slice with a second fabrication process with a second set of design rules to produce a second result; and
 - (d) means for comparing said first result and said second result to produce a third result.
14. (original): The apparatus of claim 13, wherein said slice is a RapidSlice™.

15. (original): The apparatus of claim 13, wherein said means (d) performs a hybrid analysis whereby evaluation of an element of said slice is discontinued when said element is established to be accessible in said second fabrication process.
16. (original): The apparatus of claim 13, wherein said means (d) comprises a network-distributed processing system.
17. (original): The apparatus of claim 13, wherein said third result including at least one variable that is invariant in said platform-based design.
18. (original): The apparatus of claim 13, further comprising means for modifying said slice definition based on said third result.
19. (original): The apparatus of claim 13, further comprising means for optimizing a metalization process giving a final function of said slice based on said third result.
20. (original): The apparatus of claim 13, further comprising means for modifying said first fabrication process based on said third result.
21. (original): The apparatus of claim 13, further comprising means for modifying said second fabrication process based on said third result.
22. (original): The apparatus of claim 13, further comprising means for storing said third result into a database.
23. (original): The apparatus of claim 13, further comprising means for optimizing platform architecture used to predefine said slice based on said third result.
24. (original): The apparatus of claim 23, further comprising means for optimizing temporal structure of interconnect of said platform architecture based on said third result.

25. (currently amended): A computer-readable medium having computer-executable instructions for performing a method for mapping platform-based design to multiple foundry processes, said method comprising steps of:

- (a) predefining a slice, said slice being a constrained and abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, and a transistor array of a chip;
- (b) mapping said slice onto a first fabrication process with a first set of design rules to produce a first result;
- (c) evaluating said slice with a second fabrication process with a second set of design rules to produce a second result; and
- (d) comparing said first result and said second result to produce a third result.

26. (original): The computer-readable medium of claim 25, wherein said slice is a RapidSlice™.

27. (original): The computer-readable medium of claim 25, wherein said step (d) is a hybrid analysis whereby evaluation of an element of said slice is discontinued when said element is established to be accessible in said second fabrication process.

28. (original): The computer-readable medium of claim 25, wherein said step (d) is accomplished with a network-distributed processing system.

29. (original): The computer-readable medium of claim 25, wherein said third result including at least one variable that is invariant in said platform-based design.

30. (original): The computer-readable medium of claim 25, wherein said method further comprising modifying said slice definition based on said third result.

31. (original): The computer-readable medium of claim 25, wherein said method further comprising optimizing a metalization process giving a final function of said slice based on said third result.

32. (original): The computer-readable medium of claim 25, wherein said method further comprising modifying said first fabrication process based on said third result.

33. (original): The computer-readable medium of claim 25, wherein said method further comprising modifying said second fabrication process based on said third result.

34. (original): The computer-readable medium of claim 25, wherein said method further comprising storing said third result into a database.

35. (original): The computer-readable medium of claim 25, wherein said method further comprising optimizing platform architecture used to predefine said slice based on said third result.

36. (original): The computer-readable medium of claim 35, wherein said method further comprising optimizing temporal structure of interconnect of said platform architecture based on said third result.

37. (currently amended): A computer-readable medium having stored thereon a database having a data structure, said data structure comprising:

(a) a first field containing data representing a slice definition, said slice definition being a constrained and abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, and a transistor array of a chip;

(b) a second field containing data representing a first set of design rules with which said slice definition is mapped to a first fabrication process;

(c) a third field containing data representing a second set of design rules with which said slice definition is mapped to a second fabrication process; and

(d) a fourth field containing data representing a result of computed comparison between results of said two mapping mappings.

38. (original): The computer-readable medium of claim 37, wherein said slice is a

RapidSliceTM.

39. (original): The computer-readable medium of claim 37, wherein said result of computed comparison includes at least one variable that is invariant in platform-based design used to provide said slice definition.
40. (original): The computer-readable medium of claim 37, wherein said database is used to modify said slice definition.
41. (original): The computer-readable medium of claim 37, wherein said database is used to optimiz a metalization process giving a final function of said slice definition.
42. (original): The computer-readable medium of claim 37, wherein said database is used to modify said first fabrication process.
43. (original): The computer-readable medium of claim 37, wherein said database is used to modify said second fabrication process.
44. (original): The computer-readable medium of claim 37, wherein said database is used to optimize platform architecture used to provide said slice definition.
45. (original): The computer-readable medium of claim 44, wherein said database is used to optimize temporal structure of interconnect of said platform architecture.